[19 (c20)]
A method of forming retrograde n-well and p-well regions on a substrate, comprising the steps of:
forming a first mask structure on the substrate comprised of a first thin layer on the substrate and a second thick layer on said thin layer;
removing portions of said second layer; defining an image in said second layer
carrying out n-well implants into regions of the substrate beneath said removed portions of said second layer;
removing portions of said first layer;
carrying out a first p-well implant through said first layer so that a first implant region is formed immediately below the n-well and a second implant region is formed below the first mask structure;
forming a second mask structure on the substrate having an image generally complementary to the first mask structure; and
carrying out p-well implants into regions of the substrate exposed by the second mask structure.

[20 (c21)]
A CMOS device having FETs with effective channel lengths less than or equal to approximately 0.11um formed in adjacent, retrograde nwells and pwells, wherein threshold voltages of FETs formed with approximately 1.5 um of an interface between said nwells and pwells are constant within approximately 10 mV.

[h3] Abstract of the Disclosure

[p17] A method of forming retrograde n-wells and p-wells. A first mask is formed on the substrate and the n-well implants are carried out. Then the mask is thinned, and a deep p implant is carried out with the thinned n-well mask in place. This prevents Vt shifts in FETs formed in the n-well adjacent the nwell-pwell interface. The thinned mask is then removed, a p-well mask is put in place, and the remainder of the p-well implants are carried out.

[h7] Figures